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Abstract
In this thesis, a permanent magnet synchronous motor (PMSM) speed control IC implemented by a FPGA chip is presented. This control IC contains two major intellectual properties (IP). One is the current vector control IP used in current loop of the PMSM, the other is fuzzy control IP used in speed loop of the PMSM. The current vector control IP performs the function of the coordinate transformation, the detection of quadrature encoder pulse, the current detection (A/D conversion), the space vector pulse width modulation (SVPWM), and two PI controllers. The fuzzy control IP performs the function of normalization, fuzzification, fuzzy inference, defuzzification and denormalization. Except that, this control IC also contains a bus interface IP. Therefore, the control IC can receive the external speed command and transmit the running status and dynamic information of the PMSM to external processor (such as, DSP chip) through this bus interface IP. To simplify the design and increase the precision realization, a modular design approach is proposed and a 12-bit data length with Q11 and signed 2’s complement computation in vector control IP and a 10-bit data length in fuzzy control IP are utilized. In this thesis, the Altera CycloneEP1C20 FPGA chip is used and the circuits are designed by VHDL. At last, except simulation, an experimental system which includes a FPGA-based servo board, a TMS320F24x DSK, an inverter, a rectifier, a PMSM and a set of PC has been set up and some experimental results have been provided for demonstrating the effectiveness of the proposed speed control IC.
Advisory Committee Ying-Shieh Kung - advisor

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